RESPONSE UNDER 37 CFR 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2822

PATENT APPLICATION
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:	Kyoung-Woo LEE, et al.		
Serial No.:	10/688,077	Examiner:	Guerrero, Maria F.
Filed:	October 16, 2003	Group Art Unit:	2822
Confirmation No.:	8142		
For:	INTEGRATED CIRCUIT CAPACITOR STRUCTURE		

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AMENDMENT AFTER FINAL REJECTION UNDER 37 CFR 1.116

Responsive to the Final Office Action, Paper No. 20051222, dated April 21, 2006, please amend the application as follows.

Amendments to the Claims are reflected in the listing of claims, which begins on page 2 of this paper.

Remarks/Arguments begin on page 6 of this paper.

IN THE CLAIMS

1. (Currently amended) A method of manufacturing an MIM capacitor, which includes a lower electrode, a first wiring layer that is located below or in a same level with the lower electrode and is insulated from the lower electrode, and an upper electrode that overlaps with the lower electrode and contacts the first wiring layer through a contact hole in a dielectric layer that is between the upper electrode and the lower electrode, the method comprising:

forming the dielectric layer on the entire surface of a substrate on which the lower electrode and the first wiring layer are formed;

patterning the dielectric layer to form the contact hole through which the surface of the first wiring layer is exposed, wherein patterning the dielectric layer comprises:

forming a dual hard mask (DHM) on the dielectric layer; and

etching the dielectric layer using the DHM as an etching mask; and

forming the upper electrode comprising a material to contact the first wiring layer through the contact hole,

wherein forming the DHM on the dielectric layer comprises:

forming on the dielectric layer a DHM lower layer comprising the same material that is used to form the upper electrode;

forming a DHM upper layer of a dielectric material on the DHM lower layer;

forming a photoresist pattern that defines the contact hole on the DHM upper layer;

etching the DHM upper and lower layers using the photoresist pattern as an etching mask; and

removing the photoresist pattern.

2-3. (Cancelled)

4. (Original) The method of claim 3, wherein the DHM upper layer and the dielectric layer are formed of the same material to the same thickness.

5. (Original) The method of claim 3, further comprising substantially etching away the DHM upper mask at the same time as etching the dielectric layer.

6. (Original) The method of claim 5, wherein forming the upper electrode comprises:

forming a conductive layer on the DHM lower mask and within contact hole; and

patterning the conductive layer and the DHM lower mask.

7. (Previously presented) The method of claim 2, wherein forming the DHM on the dielectric layer comprises:

forming a dielectric DHM lower layer on the dielectric layer, the DHM lower layer having an etch selectivity relative to the dielectric layer;

forming a dielectric DHM upper layer on the DHM lower layer;

forming a photoresist pattern that defines the contact hole on the DHM upper layer;

etching the DHM lower and upper layers using the photoresist pattern as an etching mask; and

removing the photoresist pattern.

8. (Original) The method of claim 7, wherein the DHM upper layer and the dielectric layer are formed of the same material to the same thickness.

9. (Original) The method of claim 7, wherein etching the dielectric layer using the DHM as an etching mask comprises:

substantially etching away the DHM upper mask at the same time as etching the dielectric layer; and

removing the DHM lower mask to expose a surface of the dielectric layer.

10. (Original) The method of claim 9, wherein forming the upper electrode comprises:

forming a conductive layer on the dielectric layer and within the contact hole; and

patterning the conductive layer to complete the upper electrode.

11-22. (Cancelled)

23. (New) A method of manufacturing an MIM capacitor, which includes a lower electrode, a first wiring layer having a top surface that is located at or below a bottom surface of the lower electrode and is insulated from the lower electrode, and an upper electrode that overlaps with the lower electrode and contacts the first wiring layer through a contact hole in a dielectric layer that is between the upper electrode and the lower electrode, the method comprising:

forming the dielectric layer on the entire surface of a substrate on which the lower electrode and the first wiring layer are formed;

patterning the dielectric layer to form the contact hole through which the surface of the first wiring layer is exposed; and

forming the upper electrode comprising a material to contact the first wiring layer through the contact hole.

24. (New) A method of manufacturing an MIM capacitor, which includes a lower electrode located above an interlayer dielectric layer, a first wiring layer that is disposed in the interlayer dielectric layer and that is below, and insulated from, the lower electrode, and an upper electrode that overlaps with the lower electrode and contacts the first wiring layer through a contact hole in a non-planer dielectric layer that is between the upper electrode and the lower electrode, the method comprising:

forming the non-planer dielectric layer on the entire surface of a substrate on which the lower electrode and the first wiring layer are formed so that the non-planer dielectric layer includes steps to cross up and over the lower electrode;

patterning the non-planer dielectric layer to form the contact hole through which the surface of the first wiring layer is exposed; and

forming the upper electrode comprising a material to contact the first wiring layer through the contact hole.

25. (New) A method of manufacturing an MIM capacitor, which includes a lower electrode, a first wiring layer that is located below or in a same level with the lower electrode

and is insulated from the lower electrode, and an upper electrode that overlaps with the lower electrode and contacts the first wiring layer through a contact hole in a dielectric layer that is between the upper electrode and the lower electrode, the method comprising:

forming the dielectric layer on the entire surface of a substrate on which the lower electrode and the first wiring layer are formed;

patterning the dielectric layer to form the contact hole through which the surface of the first wiring layer is exposed; and

forming the upper electrode comprising a single conductive layer.

26. (New) The method of claim 25, wherein the upper electrode contacts both the first wiring layer through the contact hole and a top surface of the dielectric layer.